ABSTRACT OF THE DISCLOSURE

A synchronous integrated circuit memory device including an array of memory cells. The memory device includes a clock receiver to receive an external clock signal, and a plurality of sense amplifiers, coupled to the array of memory cells, to sense data. A first portion of the data is output from the memory device in response to a first operation code bit specifying a read operation. In addition, the memory device includes a first input receiver to sample the first operation code bit in response to a first transition of the external clock signal. Furthermore, the memory device includes a second input receiver to sample a second operation code bit in response to the first transition of the external clock signal. The second operation code bit indicates whether precharging the plurality of sense amplifiers occurs automatically after the data has been sensed. Moreover, the memory device includes a plurality of output drivers to output the portion of the data synchronously with respect to the external clock signal.